

## Micro and Nano Electronics

1. P. N. Kondekar and B. Awadhiya, "Effect of parameter variation in UTBB FDSOINCFET," *2017 Joint IEEE International Symposium on the Applications of Ferroelectric (ISAF)/International Workshop on Acoustic Transduction Materials and Devices (IWATMD)/Piezoresponse Force Microscopy (PFM)*, Atlanta, GA, 2017, pp. 45-47. doi: 10.1109/ISAF.2017.8000208
2. S. Dubey and P. N. Kondekar, "Doping dependent stacked channel FinFET for multiple threshold voltage applications," in *International Conference on Emerging Electronics*, Dec.2016.
3. A. Gedam, S. Pandey, S. Yadav, K. Nigam, D. Sharma, P. N. Kondekar, "Realization of Junctionless TFET based Power Efficient 6T SRAM Memory Cell for Internet-of-Things Applications," in *Smart Innovation, Systems and Technologies, Communications in Computer and Information Science*, Springer, pp. 1-8, 2017.
4. Jyoti Patel, Priyanka Suman, AlemienlaLemtur and Dheeraj Sharma, Performance Booster Electrical Drain SiGeNanoWire TFET (ED-SiGe-NW-TFET) with DC Analysis and Optimization, 3rd International Conference on Information and Communication Technology for Intelligent Systems (ICTIS 2018), Springer Smart Innovation, Systems and Technologies (SIST), 6-7 April. 2018 (Accepted).
5. AlemienlaLemtur, Priyanka Suman, Jyoti Patel and Dheeraj Sharma, Significance of hetero-junction in charge plasma gate all around TFET: An investigation, 3rd International Conference on Information and Communication Technology for Intelligent Systems (ICTIS 2018), Springer Smart Innovation, Systems and Technologies (SIST,) 6-7 April. 2018 (Accepted).
6. S. Yadav, D. Sharma, Mohd. Aslam and D. Soni., A Novel Analysis to Reduce Leakage Current in Charge Plasma Based TFET at INDICON is organized by IEEE Uttar Pradesh Section, and going to be held from 15th 17th December 2017, at IIT Roorkee, Uttarakhand India.
7. D. S. Yadav, D. Sharma, S. Tirkey, D. Soni, D. G. Sharma and S. Bajpai., A Comparative Study of GaP/SiGe heterojunction double gate Tunnel Field Effect Transistor going to be held at the IEEE International Symposium on Nanoelectronics and Information Systems (IEEE iNIS-2017), to be held from 18<sup>th</sup> 20<sup>th</sup> Dec, 2017, at OIST Bhopal, India. )
8. D. Soni, D. Sharma, S. Yadav, Mohd. Aslam and D. S. Yadav., Gate metal work function engineering for the improvement of electrostatic behaviour of doped tunnel field effect

transistor IEEE International Symposium on Nanoelectronics and Information Systems (IEEE iNIS-2017), to be held from 18<sup>th</sup> to 20<sup>th</sup> Dec, 2017, at OIST Bhopal, India. )

9. D. S. Yadav, D. Sharma, D. G. Sharma and S. Bajpai., High Frequency Analysis of GaAsP/InSb Hetero Junction Double Gate Tunnel Field Effect Transistor IEEE's 3rd International Conference for Convergence in Technology (I2CT), sponsored by IEEE Bombay Section, going to be held from 7<sup>th</sup> to 9<sup>th</sup> April, 2018, at Hotel Gateway (TAJ), Hinjewadi, Pune, Maharashtra, India.
10. Sarthak Gupta, Kaushal Nigam, Sunil Pandey, Dheeraj Sharma and P N Kondekar "Performance Improvement of Heterojunction Double Gate Drain Overlapped TFET using Gaussian Doping" 5th Berkeley Symposium on Energy Efficient Electronic Systems and Steep Transistors Workshop to be held on October 19-20, 2017, on the campus of the University of California, Berkeley, USA.
11. Dheeraj Sharma, Bhagwan Ram Raad, Sukeshni Tirkey "Channel Engineered Tunnel FET for Reduced Ambipolar Nature" 5th Berkeley Symposium on Energy Efficient Electronic Systems and Steep Transistors Workshop to be held on October 19-20, 2017, on the campus of the University of California, Berkeley, USA.
12. S. Tirkey, D. S. Yadav and D. Sharma, Controlling Ambipolar Behaviour and reducing radio frequency performance of Hetero- Junction Double gate TFET by Dual work function, Hetero gate dielectric and Gate Underlap: Assessment and Optimization, IEEE International Conference on Information Communication Instrumentation and Control (ICICIC -2017) held from 17<sup>th</sup>-19<sup>th</sup> Aug, 2017, at Medi-caps University Indore India.
13. D. S. Yadav, D. Sharma, R. Agrawal, G. Prajapati, S. Tirkey, B. R. Raad, and V. Bajaj, Temperature based performance analysis of doping-less Tunnel Field Effect Transistor, IEEE International Conference on Information Communication Instrumentation and Control (ICICIC -2017) held from 17<sup>th</sup>-19<sup>th</sup> Aug, 2017, at Medi-caps University Indore India.
14. Pooja Yadav, Anchala Priya, Sachin Taran, Varun Bajaj, Dheeraj Sharma " Discrimination of alcohol and normal EEG signal using EMD" 4th International Conference on signal processing and integrated networks (SPIN) 2017.
15. S. Taran, V. Bajaj, D. Sharma, TEO Separated AM-FM Components Used for Identification of Apnea EEG Signals, 2nd IEEE International Conference on Signal and Image Processing (ICSIP 2017) held from Aug, 4-6, 2017, at NTU@one-north, Singapore,.
16. S. Walde, P. Rani, V. Bajaj, and D. Sharma, Time Frequency Image based Features for detection of Focal EEG Signals, IEEE International Conference on Signal processing and

communication (ICSC 2016) held from Dec, 26-28 2016, at Jaypee Institute of Information Technology Nodia, U.P held India.

17. S. Pandey, P. N. Kondekar, K. Nigam, and D. Sharma, "A 0.9V, 3.1-10.6 GHz CMOS LNA with high gain and wideband input match in 90 nm CMOS process," 13<sup>th</sup> IEEE Asia Pacific Conference on Circuits and Systems (APCCAS), Jeju, South Korea, 25-28 Oct. 2016, pp. 1-4.
18. B. R. Raad, R. K. Sonkar, and P. N. Kondekar, "Transformer oil age determination using long period grating," workshop on recent advancement in photonics 2015, IISC Bangalore, 16-17 Dec, 2015.
19. K. Nigam, S. Pandey, P. N. Kondekar, and Dheeraj Sharma, "Temperature sensitivity analysis of polarity controlled electrically doped hetero-TFET," 12th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME), June 2016.
20. D. S. Yadav, D. Sharma, B. R. Raad and V. Bajaj, Dual Workfunction Hetero Gate Dielectric Tunnel Field-Effect Transistor Performance Analysis, IEEE international conference on advanced communication control and computing technologies (ICACCT 2016) held from May, 25-27 2016 at Ramanathapuram, Tamilnadu, India
21. B. R. Raad, D. Sharma and P. Kondekar, "Dual work function tunnel field-effect transistor with shifted gate for ambipolar suppression and ON current improvement," International Conference on Computational Techniques in Information and Communication Technologies (ICCTICT), March 2016.
22. S. Kale, S. Banchhor and P. N. Kondekar, "Impact of underlap channel on analog/RF performance of dopant segregated Schottky barrier MOSFET on ultra thin body SOI," International Conference on Emerging Trends in Engineering, Technology and Science (ICETETS-2016), Tamilnadu, India, Feb. 2016.
23. R. Sinha, S. Singh and P. N. Kondekar, "Silicon Nanowire Gate-All-Around Junctionless Tunnel FET with Bipolar Action," 18th international workshop on physics of solid state devices, (IWPSD) 2015.
24. A. Singh, S. Singh and P. N. Kondekar, "Effect of Germanium Mole fraction Variation on Bipolar Charge Plasma Transistor," 18th international workshop on physics of solid state devices, (IWPSD) 2015.
25. S. Singh, A. P. Singh, and P. N. Kondekar, "Hetero Gate PNIN Tunnel Field Effect Transistor with enhance device performance", 4th Student's Conference on Engineering and Systems 2015.
26. A. P. Singh, S. Singh, P. N. Kondekar, P. Jharia, P. Kumar, "Structural Analysis & Mathematical Modeling of Gate Inside Organic Field Effect Transistors (GI-OFET) - A Novel Device Structure", 4th Student's Conference on Engineering and Systems 2015.

27. A. Naugarhiya and P.N. Kondekar, "Optimized process design flow for fabrication of superjunction VDMOS for enhanced RDSON," 11th ISETC-2014, Timisoara, Romania.
28. P.N. Kondekar and A. Naugarhiya, "AC and transient analysis of SJ VDMOS," 11th ISETC-2014, Timisoara, Romania.
29. P. N. Kondekar, and A. Naugarhiya, "AC and Transient Analysis of SJ VDMOS" ICEBEA 2014 Dubai.
30. S. Kale, and P. N. Kondekar, "Impact of underlap channel on the performance of DG SB-MOSFET with Si<sub>3</sub>N<sub>4</sub> spacer layer," IEEE International conference on Electron Devices and Solid-State Circuits, Chengdu, China, 2014.
31. S. Banchhor, S. Kale and P. N. Kondekar, "Influence of underlap gate length on analog/ RF performance of pocket doped Schottky barrier MOSFET," 2nd IEEE International Conference on Electronics & Communication systems (ICECS-2015), pp. 1152-1155, 26-27 February, 2015, Coimbatore, India.
32. S. Kale, S. Banchhor and P. N. Kondekar, "Performance study of high-k gate & spacer dielectric dopant segregated Schottky barrier SOI MOSFET," 2nd IEEE International Conference on Electronics & Communication systems (ICECS-2015), pp. 1142-1145, 26-27 February, 2015, Coimbatore, India.
33. S. Singh, P. Kumar and P. N. Kondekar, "Transient analysis & performance estimation of gate inside junctionless transistor (GI-JLT)," International Journal of Electrical, Computer, Electronics and Communication Engineering, vol.8, no.10, World Academy of Science, Engineering and Technology, pp. 1553-1557, 2014.
34. I. Agrawal and P.N. Kondekar, "Performance analysis of tunnel field effect transistor using charge plasma concept," 10<sup>th</sup> IEEE International Conference on Electronic Devices and Solid State Circuits, (EDSSC-2014), China, 2014.
35. I. Agrawal, and P.N. Kondekar, "Drain improvement using spacer and charge plasma concept in T-FET," 18th IEEE International Symposium on Consumer Electronics (ISCE-2014), South Korea, pp.1-2, 2014.
36. S. Singh, P. Pal, R. Mittal, A. Tamia, and P.N. Kondekar, "Silicon on ferroelectric tunnel FET (SOF-TFET) for low power application," IEEE International conference on Emerging electronics (ICEE-2014), IISc Bangalore, 4-6 Dec, 2014.
37. P. Kumar, S. Singh and P. N. Kondekar, "Transient analysis & performance estimation of gate inside junctionless transistor (GI-JLT)," in 24th GLSVLSI, Houston, Texas, USA, pp 235-236, 2014.
38. A. Dixit, S. Singh and P. N. Kondekar, "Transient analysis of lateral impact ionization MOSFET (LIMOS)," in the international conference on convergence of technology Pune, 2014.

39. A. Dixit, S. Singh, P. N. Kondekar and Pankaj Kumar "Performance analysis of lateral impact ionization MOS(LIMOS)," in IEEE conference Techsym 2014, IIT Kharagpur, India, 2013.
40. A. Naugarhiya and P. N. Kondekar, "Electrical characteristics comparison between process and device structures of super junction VDMOS," 2013 International Conference on Control, Automation, Robotics and Embedded Systems (CARE), 16-18 Dec. 2013.
41. I. Agrawal, P.N. Kondekar and Sumit Kale, "Performance analysis of tunnel FET," in IEEE International Conference on Circuit, Control and Communication (C-CUBE 2013), at Bangalore, December 2013.
42. P. Kumar, C. Sahu, A. Shrivastava, P. N. Kondekar, and J. Singh, "Characteristics of gate inside junctionless transistor with channel length and doping concentration," in IEEE International conference on Electron Devices and Solid-State and Circuits (EDSSC13), Hong Kong, Polytechnic University, 2013.
43. P. Kumar, S. Singh, P. N. Kondekar, and A. Dixit, "Digital and analog performance of gate inside p-type junctionless transistor (GI-JLT)," in CIMSIm2013, IEEE 5th International Conference on Computational Intelligence, Modeling and Simulation (CIMSIm2013), Seoul, Korea, pp. 394-397, 2013.
44. P. Kumar, S. Singh, P. N. Kondekar and I. Agrawal, "Characteristic and sensitivity of gate inside junctionless transistor (GI-JLT)," in 20th IEEE International Conference on Electronics, Circuits, and Systems (ICECS-2013), UAE, pp.256-259, 2013.
45. S. Pandey, S. Agrawal, Jawar Singh, and P.N. Kondekar, "A low-power and compact CMOS based CDTA and its application," 17th International Symposium on VLSI Design and Test MNIT Jaipur, 2013.
46. P. Yadav, D. Kumar, P.N. Kondekar and J. Singh, "Structural analysis of optimized low voltage organic field effect transistor based on pentacene," in International Conference on NUiCONE, 2012.
47. C. Sahu, J. Singh and P.N. Kondekar, "Investigation of ultra-thin BOX junctionless transistor at channel length of 20 nm," IEEE International conference on Electron Devices and Solid-State and Circuits (EDSSC'13) Hong Kong, 3-5 June 2013.
48. A. Chakraborty, P.N. Kondekar and M. Yadav, "Drive current boosting and low sub-threshold swing obtained by layer in double-gate tunnel FET," in Proc. of ESciNano 2012, Malaysia.
49. D. Kumar, P. Yadav, P.N. Kondekar and J. Singh, "High performance organic field effect transistor with tri-gate," in IEEE International Conference on Intelligent System, Modeling & Simulation-2013.

50. D. Kumar, P. Yadav, P.N. Kondekar and J. Singh, "Analysis and comparison of organic field-effect transistor with different dielectric insulators," in IEEE International Conference on Intelligent System, Modeling& Simulation -2013.
51. P. Yadav, D. Kumar, P.N. Kondekar and J. Singh, "High performance pentacene-based organic transistor with HfO<sub>2</sub>-Al<sub>2</sub>O<sub>3</sub> as dielectrics," in the International Conference of ICMENS, 2012.
52. P. Wakhradkar, A. Naugarhiya and P. N. Kondekar, "Analysis of Anisotropic 4H-SiC SJ Drift Layer," 2nd ET2ECN-2014, SVNIT. Surat India.