

## Course Content

- ❖ Overview of classical semiconductor devices and technologies, and their evolution.
- ❖ Issues and challenges of classical semiconductor devices in the nano-meter regime, such as process variability, reliability and aging phenomena.
- ❖ The emergence of non-classical devices, working principal and their potential applications including VLSI for DSP.
- ❖ Specific emphasis on potential emerging devices, such as FinFETs, Junctionless FETs, dopingless FETs, re-configurability of FETs and variety of tunnel FETs (TFETs), and MEMRISTOR.
- ❖ Compact SPICE modeling of these devices and Monte Carlo simulations for uncertainty analysis.
- ❖ Memory technologies such as SRAM, DRAM, RARM and FLASH.
- ❖ Hand-on training of TCAD/EDA tools and HDL.

## About the City

The city of Jabalpur is known and considered as Sanskardhani, a “Cultural Center Place”. It is a place of great historical and cultural importance. This Cultural capital of Madhya Pradesh is situated on the bank of the holy Narmada and Famous for Dhuandhar Falls and Marble Rocks in Bhedaghat, Hanumantal Bada Jain Mandir, Madan Mahal Fort, Rani Durgawati Museum. Simultaneously it is keeping pace with modern advanced knowledge. Jabalpur is an important junction for the Indian Railways. Jabalpur is a large Defence and Military Center. Jabalpur is also known for housing spiritual leaders Maharishi Mahesh Yogi and Bhagwaan Shri Rajneesh (Osho). This vibrant city with multiple dimensions of knowledge and liberation has a magnetic attraction for people all over the world. The Jageshwar Nath Shiv Temple at Bandakpur, near Damoh, Kundalpur Jain Teerth Kshetra, near Damoha, Vishnu-Varaha Temple, Majholi, Pench National Park, Kanha Tiger Reserve, Bandhavgarh National Park are attractions near Jabalpur city.

## Route to Jabalpur

The city of Jabalpur is well connected by road, rail and air with all the important places of India. Regular flights are provided by Air India & Spice Jet. Daily services are available to Bhopal, Delhi, Hyderabad and Mumbai. Jabalpur Junction has Direct Service to Mumbai, New Delhi, Bhopal, Kolkata, Nagpur, Patna etc. The IIITDM campus is only 10 Km from Jabalpur railway station 5.5 Km from the Dumna airport.

## About the PDPM IIITDM

IIITDM Jabalpur was established in 2005 with a focus on education and research in IT enabled Design and Manufacturing. Since its inception, PDPM IIITDM Jabalpur has been playing a vital role in producing quality human resources for contribution in India’s mission of inclusive and sustainable growth. The Institute offers undergraduate, post graduate and



PhD programmes in Computer Science and Engineering, Electronics and Communication Engineering, Mechanical Engineering, Design and PhD programmes in Mathematics and Physics. Under IIIT act, the Institute has been declared an Institute of National Importance in January 2015. The Institute campus is being developed on 250 acres of land close to Dumna Airport, Jabalpur.

## Course Material

Hard / soft copies of the lecture notes/presentations will be made available to participants at the end of lecture/presentation.

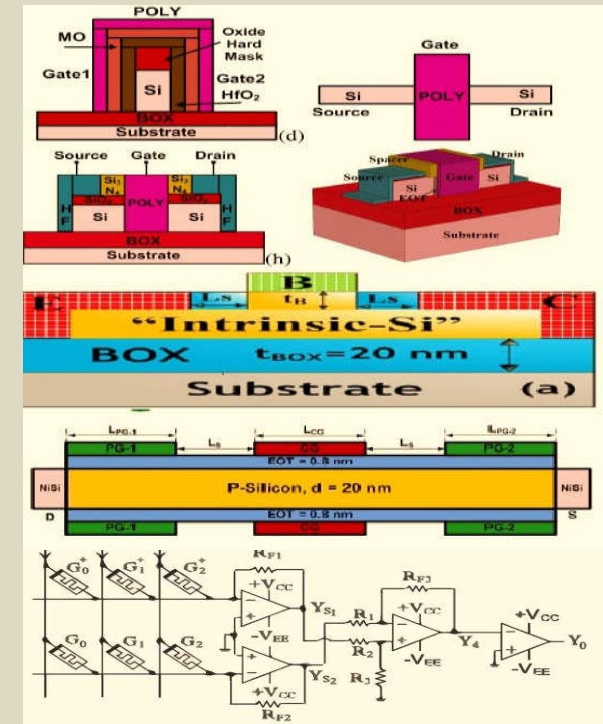


**AICTE (QIP) Sponsored  
Short Term Course On**



**Emerging Nano-electronic Devices,  
Modeling, Simulations and Applications**

**June 26-30, 2017**



**Organized by:  
Discipline of Electronics and  
Communication Engineering, PDPM  
IIITDM Jabalpur, MP**

## Course Coordinators

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## AICTE (QIP) Sponsored Short Term Course on

*Emerging Nano-electronic devices, Modeling, Simulations and Applications*  
June 19-23, 2017

### About the course and objectives:

Since last five decades semiconductor industry has been witnessed a tremendous growth and impacted the life of millions of people across the globe. A driving force behind this industrial revolution is the development of new electronic devices to meet the future requirements. In this course, we aim to provide participants detailed background about the evolution of semiconductor industry and what are the leading technologies currently being used and potential technologies to meet the future requirements, as per the international technology roadmap for semiconductors (ITRS). In broad, emphasis will be on CMOS technology and how it can sustain the future challenges.

The course is intended to young researchers and faculty members having general introductory background of semiconductor devices.

### Who Can Attend?

All existing faculty members working in the field of Microelectronics/VLSI are primarily targeted for this short duration course work. **No course fee is charged for participants sponsored by the AICTE approved Institutions.** Participants from Governments Departments and Industries are eligible, provided they meet their T.A.

and D.A. and pay a course fee @ Rs. 2500/- and Rs. 5000/-, respectively. The registration fee to be paid online in Allahabad Bank, Branch Mehgawan, Jabalpur (IFSC Code ALLA0212433) Account No. 50388395415 in favor of QIP PDPM IIITDM Jabalpur through any nationalized bank and payable at Jabalpur. The fee includes a kit containing the study material, tea and snacks.

### How to Apply?

By Email – Scanned copy of the filled in application form duly endorsed by the forwarding authority to be mailed at [stc.qip@gmail.com](mailto:stc.qip@gmail.com) by **June 15, 2017**. Application format is given in this brochure. Accommodation and local hospitality will be provided to the selected candidates from the AICTE approved institutions in the Institute guest house/hostels.

### Important Dates

Last Date of Registration: **June 15, 2017**

Intimation of Selection: **June 15, 2017**

Course Dates: **June 26-30, 2017**

Note: The selected participants have to pay online Rs. 1000/- from any nationalized bank in Allahabad Bank, Branch Mehgawan, Jabalpur (IFSC Code ALLA0212433) Account No. 50388395415 in favor of QIP PDPM IIITDM Jabalpur as a security deposit for confirmation of their participation. The security money will be returned back to the participant account only if he/she joins the course.

### Financial Assistance

Limited number of participants (30) from the AICTE approved engineering institutions will be eligible for to and fro train fare via shortest route in III AC class and free lodging and boarding in the Institute guest house/hostels during course period. Candidates attending the course in full only will be eligible for TA. For all other participants no TA will be paid.

Website: [www.iiitdmj.ac.in](http://www.iiitdmj.ac.in)

## Application for Registration

### Emerging Nano-electronic Devices, Modeling, Simulations and Applications

June 26-30, 2017

1. Name .....
  2. a) Age..... b) Sex: M/F.....
  3. Designation .....
  4. Organisation .....
  5. Address for correspondence  
.....  
.....  
E-mail:.....  
Phone/Mobile.....
  6. Highest Academic Qualification.....
  7. Specialisation .....
  8. Experience (in years)  
a) Teaching: .....
  - b) Industrial. ....
  9. Amount of T.A. required as per entitlement mentioned in the brochure (only for AICTE approved college teachers): .....
  10. Details (Reference No etc.) of fee/security deposit: .....
- Please register me for the AICTE sponsored short term course on “Emerging Nano-electronic Devices, Modeling, Simulations and Applications” to be held at IIITDM Jabalpur.  
Date.....  
Place ..... Signature of the Applicant

### SPONSORSHIP

Prof./Dr./Mr./Ms./Mrs./..... is an employee of our institute and his/her application is hereby sponsored. The applicant will be permitted to attend the AICTE sponsored short term course on “Emerging Nano-electronic Devices, Modeling, Simulations and Applications” to be held at IIITDM Jabalpur during June 26-30, 2017, if selected.

Date: ..... Signature of Sponsoring Authority  
Designation:  
Official Seal: